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ELECTRONIC MULTIPLEX SWITCH

J-4939

29 JUNE 1965

REV. A - 15 OCTOBER 1965

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APPROVED:	f ÷

EXHIBIT A

ELECTRONIC MULTIPLEX SWITCH

A completely solid state electronic multiplexer switch is proposed which will be electrically and mechanically a direct plug-in replacement for the present electromechanical unit.

The new unit offers all the advantages of solid state circuitry including the following:

- 1. Much greater lifetime no moving parts
- 2. High reliability
- 3. Reduced RFI generated
- 4. Substantial decrease in weight
- 5. Ease of maintenance
- 6. Ease of troubleshooting and repair
- 7. Rapid and reliable synchronizing from master drive
- 8. Constructed of the same standard solid state components used in EMR-AGE, hence simplified sparing and logistics
- 9. Operates continuously in ambient temperatures up to 70°C (158°F) with no cooling, and in much higher ambient temperatures with proper cooling.
- 10. Basic MPX switch is a single deck, 45 contact unit.

 Additional 45 contact decks may be added easily, operating from the same drive circuitry. Up to 3 decks can be accommodated in the same dimensions as the present mechanical switch. By adding length, up to 5 decks can be driven from the same drive circuits.

- 11. Voltage drop through the solid state switching elements is negligible (in the microvolt region) and will not degrade the overall system scaling accuracy.
- 12. Insensitive to transients and overvoltages.

The electronic MPX switch offers notable advantages in rapid synchronization. If a noise pulse put the multiplexer out of sync, the mechanical unit could generate as many as 48 scans of erroneous data until synchronization was reachieved. The solid-state electronic switch will be completely resynchronized at the end of each scan.

The block diagram of the electronic multiplexer is shown in Figure 1. The sequence logic puts a gate pulse on one of its output lines each time a clock pulse is received. The gate progresses sequentially down the lines, returning to 1 after 47 or whenever a sync pulse is received.

The analog gates transmit their inputs only when they receive a gate pulse. Thus the forty-seven inputs are sampled sequentially to make up the multiplexer output.

In packaging this unit the sequence logic and power regulators will be mounted on one set of printed circuit boards. The analog gates will be mounted on other boards. A multi-output multiplexer is easily achieved with this arrangement by wiring the outputs of the sequence logic boards to another set of analog gate boards. This would serve the same function as adding a new deck to the electromechanical multiplexer.

A flip-flop ring counter will be used for the sequence logic. Only one stage at a time is in the set state. Each clock pulse would shift the set state one stage down the ring. The ring closes on itself so that the number 1 stage follows the number 47 stage. Whenever a sync pulse is received the ring is reset so that only the number 1 stage is set (if it is not already in this position). Three stages of logic are used to make the ring stay in positions 46 and 47 for two counts each. All the electronics for the sequence logic are integrated circuits to keep weight and size to a minimum and to provide the highest reliability.

- The analog gate will be a field effect transistor.

 These units are packaged in a T05 transistor case. When the gates are in the open state the leakage current is of the order of a few nanoamperes. When they are closed, the off-set voltage is of the order of a hundred microvolts. The dynamic impedance in the conducting state is several hundred ohms which is negligible compared to a 100K load.
- The analog gates conduct continuously only when ground potential is applied to the gating input. The outputs of the sequence logic will be used to gate the analog gates.

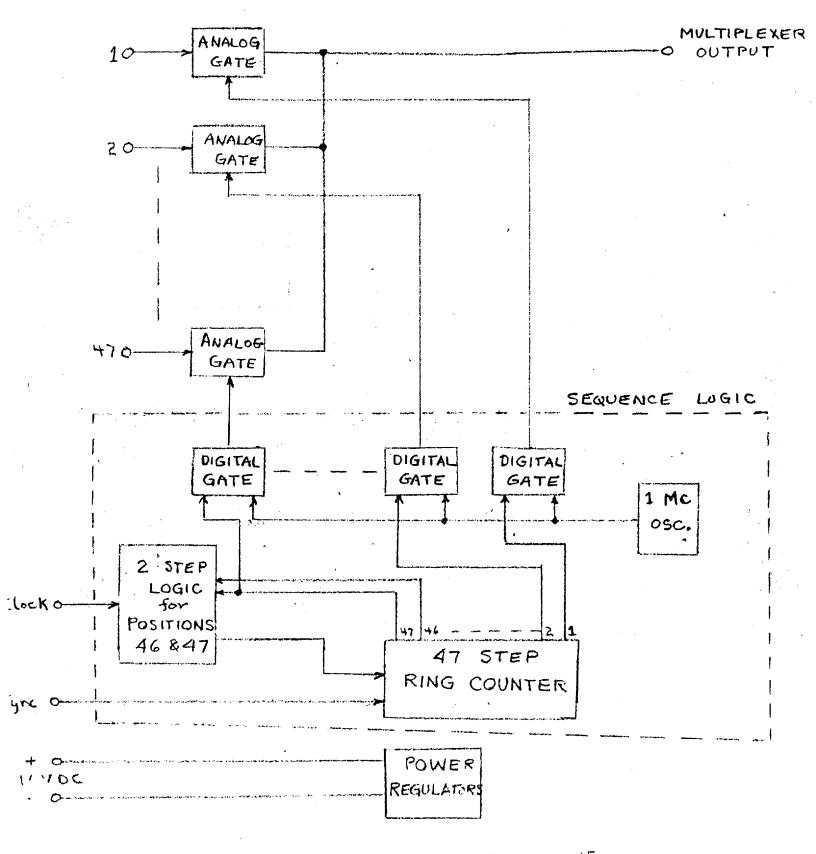
 The 47 AND gates needed would be integrated quadruple two input logic gates.

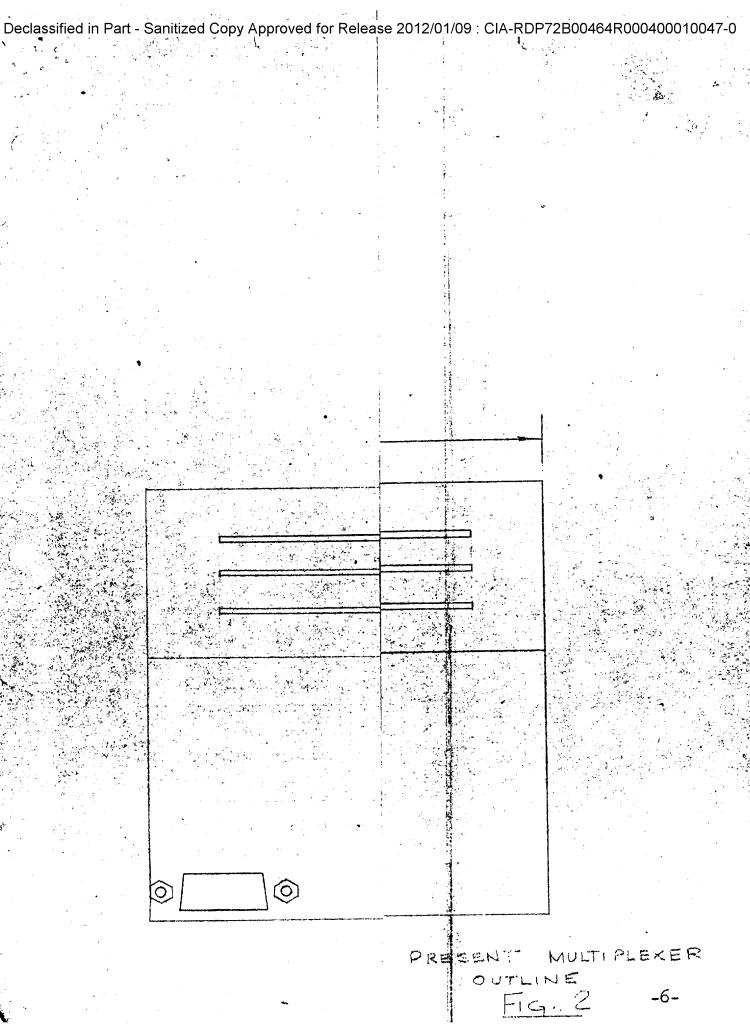
The above design for the multiplexer has the advantage of not needing an output buffer stage. The low leakage current of the analog gates allow them to be tied directly together. Their low dynamic resistance and offset voltage eliminates the need for an output amplifier.

An outline drawing of the present mechanical multiplexer is shown in Figure 2. This package is not the optimum one for a solid state unit. It appears doubtful that much of a reduction in volume can be achieved and still maintain the same physical connector configuration. If the connectors could be moved slightly the volume would probably be reduced substantially. On the assumption that the connectors cannot be moved, Figure 3 shows a possible packaging arrangement for a solid-state double deck multiplexer in the same package as a mechanical single deck unit.

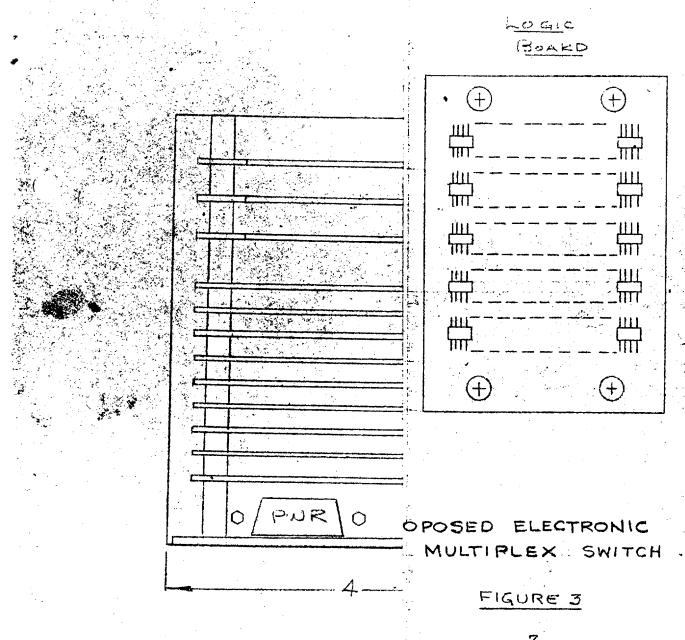
The solid state unit will be considerably lighter than the old mechanical multiplexer, cutting the weight approximately in half. The solid state multiplexer will also be extremely reliable. The estimated mean time between failure of the system described above would be in excess of 4,000 hours at 70°C, increasing substantially at lower operating temperatures. High reliability parts are used throughout.

PROPOSED ELECTRONIC MULTIPLEX
SWITCH BLOCK DIAGRAM





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FIGURE 4

MULTIPLEX SWITCH PROPOSAL - J-4939

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ANALYSIS

ECP-1940-2

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DIRECT LABOR CLASS	TOTAL HOURS		A LABOR CLASS B	TOTAL LABOR
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TECHNICIANS	2250	8857		8857
PUBLICATIONS	100	280		280
ESIGN AND DRAFTING	1660	5662		5662
SHOP	570		1829	1829
ELECTRICAL ASSEMBLY	2570		7656	7656
NSPECTION	550		1663	1663
MPC Adm SARES XXXX RESOURANCES	920		34.04	3404
PACKAGING AND SHIPPING	20	56		56
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(5) GENERAL AND	\$ 11228			
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(7) PLANNED PRO	FIT OR FEE	8 % OF ES	TIMATED COST, (6)	\$ 12875
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